BIMA Memoranda Series # 24

A PROPOSAL FOR A DIGITAL DELAY LINE SYSTEM AT HAT CREEK

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July 6, 1992

Introduction

Long baseline extensions to the Hat Creek array will require much longer delays than are currently available with the analog delay system. I have considered various alternatives, such as large coaxial cables, fiber-optic lines, or acoustic delays, and have concluded that digital delays are probably the cheapest and most practical. I'm not familiar enough with the system to assess the physical problem involved with the installation of the proposed delay system. This may be a major problem that will have to be addressed later.

The digital delay system would involve one board per antenna inserted into the 50 MHz signal paths just ahead of the correlator inputs. It would insert identical delays into each of the 64 bit streams [32 channels x 2-bits] which carry the data from each antenna. The system would provide the delays needed for the correlators; the analog system could continue to provide delays for the continuum receiver. Of course, the continuum receiver could not then be used with the long baseline extensions to the array.

The delay boards could be constructed and tested at Maryland. A reasonable time for their installation into the Hat Creek system would be next summer (1993) so work on this system would have no impact upon the effort to get the six element array into operation. Under this schedule we would not have the longer delays available for any work with the long baseline extensions next spring and any such work would have to be confined to observations of maser sources. We need to make a decision in the next few months concerning the type of delay system that will eventually be implemented so that long lead-time devices can be ordered. The purpose of this memo is to simulate the discussion necessary for making such a decision.

Circuit Description

A diagram of the proposed circuit is shown in Figure 1. It is a simplified version of the circuit that we used at Clark Lake where forty-eight such circuits operated faultlessly for many years. The bits are read from one RAM while they are being written into another one. After a delay of the appropriate number of clock cycles, the RAMs are alternated. The memory swapping cycle is generated by loading a down counter with the actual delay, counting down, toggling a memory select flip-flop, and resetting the counter when it reaches -1. If the outputs of the RAMs cannot be disabled without disabling the chip altogether, a

switch may be necessary to select the RAM being read. Flip-flops at the input and output maintain timing.

Two RAMs are required per bit stream but the RAMs are normally four bits wide so each antenna would require 32 RAMs. These RAMs would all be addressed in parallel so only one set of addressing and memory swapping circuitry is needed. Of course, only eight RAMs would be required if they could be operated at 200 MHz, but I feel that the ease of operation at 50 MHz justifies the use of the extra chips.

Operating at 50 MHz, this circuit would provide delay increments of 20 ns. RAMs 512 bits long would provide a total delay of 10,240 ns. This would almost certainly be sufficient but the extra cost of 1024-bit RAMs is so trivial that I propose that they be used. The 20,480 ns delay that they provide should be sufficient for any conceivable future experiment.

The 20 ns delay increment is too crude to maintain coherence across the 25 MHz bandwidths. Finer delay increments could be easily obtained with short analog steps or by shifting the 50 MHz control signal to the distributer multiplexer in 5 ns steps by means of a two-bit, 200 MHz down-counter. The current 3.91 ns delay increment results in a maximum coherence loss of 1.56% and an average loss of 0.13% [assuming a uniform 25 MHz bandwidth]. For a 5 ns increment the corresponding losses are 2.55% and 0.22%.

Cost Estimate

The 32 RAMs needed for each antenna should fit on one VME board. I have estimated the cost of the chips and the VME board needed for each antenna. I do not estimate the cost of installing the boards and providing the necessary power and the control signals.

The boards could be built and tested to the level of bits- out verses bits-in by the electronics development group here at Maryland. For each antenna the cost of the chips is $2500 [32 RAMs at $70 each amounts to $2240] and the completed board should cost $3500 to $4000 at a maximum. In addition it would cost the electronics development shop an extra $8000 to $9000 to produce the first board. This one-time cost is for detailed design and development and for procurement of the necessary test equipment and a VME cage. These costs could be reduced if the items could be borrowed or rented economically. In any event, I believe that this solution to the delay problem would be more economical and satisfactory than the alternatives.

RAM DELAY

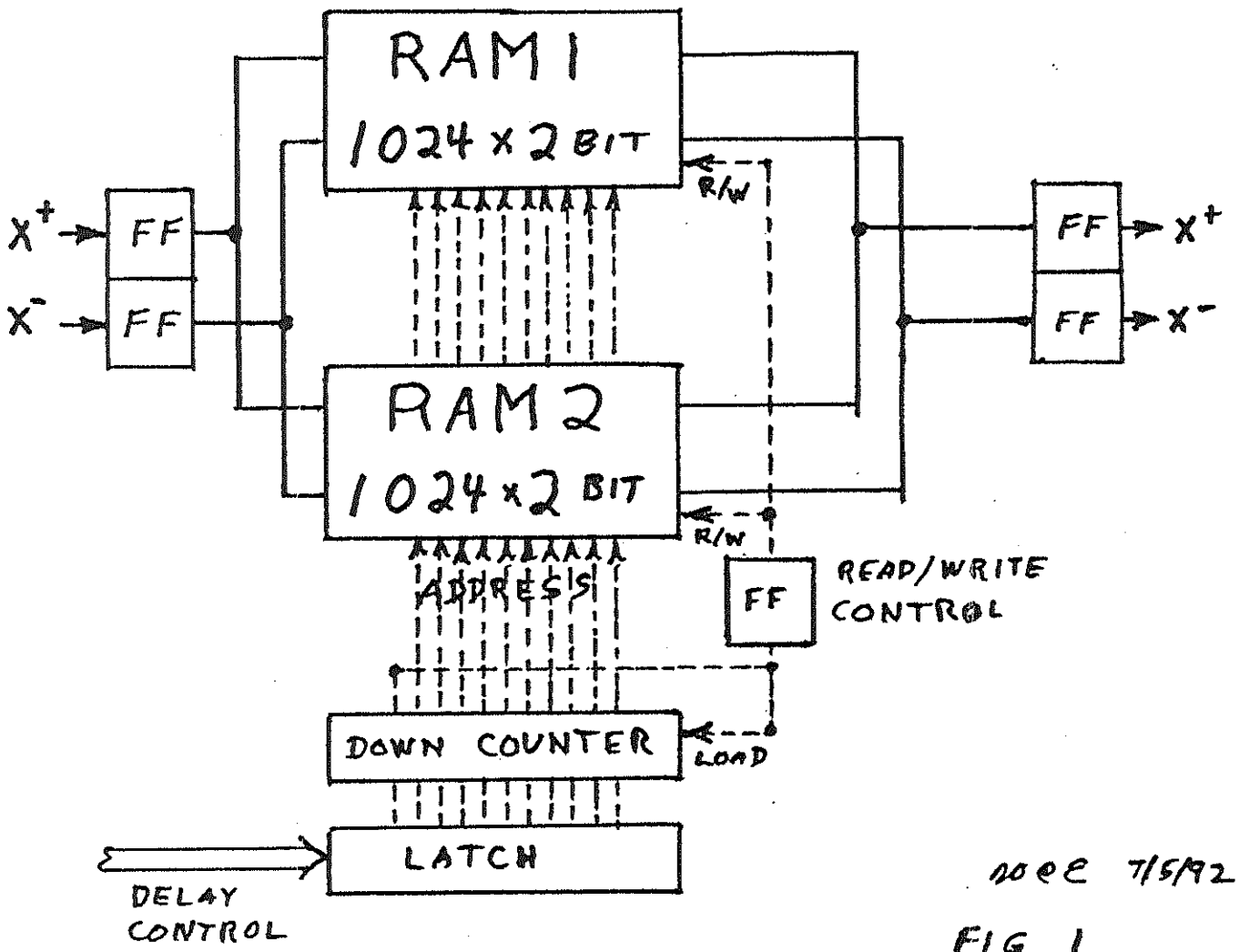

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FIG. 1